alterations and modifications as fall within the true spirit and scope of the invention.

12 Cm I claim:

IN THE CLAIMS

1. A high-voltage MOS transistor comprising an insulated-gate field-effect transistor, and a double-sided junction-gate field-effect transistor connected in series, said transistors being united in one structure.

2. In a high-voltage MOS transistor having a source, a drain, an insulated gate device for controlling current flow between the source and the drain, an extended drain region in series between the insulated-gate device and the drain, said extended drain region being formed on material having a conductivity-type opposite that of the extended drain region, and wherein the improvement comprises a layer of material on top of the extended drain region having a conductivity-type opposite that of the extended drain region, and wherein the improvement comprises a layer of material on top of the extended drain region having a conductivity-type opposite that of the extended drain region, said top layer of material and said material beneath the extended drain region being interconnected with the source for applying a reverse-bias voltage whereby current flow through the extended drain region can be pinched off by depletion from both sides adjacent the opposite conductivity-type materials.

3. A high-voltage MOS transistor comprising a source, a drain, an insulated gate device for controlling current flow between the source and the drain, an extended drain region in series between the insulated gate device and the drain, said extended drain region being formed on material having a

conductivity-type opposite that of the extended drain region, and a layer of material on top of the extended drain region having a conductivity-type opposite that of the extended drain region, said top layer of material and said material beneath the extended drain region being interconnected with the source for applying a reverse-bias voltage whereby current flow through the extended drain region can be pinched off by depletion from both sides adjacent the opposite conductivity-type materials.

4. The high-voltage MOS transistor of claim 1 further including,

another high-voltage MOS transistor of opposite conductivity-type forming a complementary pair on the same chip.

5. The high-voltage MOS transistor of claim 2 wherein,

said layer on top of the extended drain region is an ion-implantation.

6. The high-voltage MOS transistor of claim 5 wherein,

said top layer has a depth of one-micron or less.

7. The high-voltage MOS transistor of claim 5 wherein,

said top layer has a doping density higher than 5 x $10^{16}/cm^3$ so that the mobility starts to degrade.

8. The high-voltage MOS transistor of claim 3 wherein,

said extended drain is made of n-type conductive material and said top layer is made of p-type conductive material.

9. The high-voltage MOS transistor of claim 3 wherein,

said extended drain is made of p-type conductive material and said top layer is made of n-type conductive material.

10. The high-voltage MOS transistor of claim 9 wherein,

said transistor is embedded in a well of n-type conductive material in a substrate of p-type conductive material, and further including a complementary high-voltage MOS transistor having an extended drain of n-type conductive material embedded in the substrate.

11. The high-voltage MOS transistor of claim 3 wherein,

both the extended drain region and the top layer of material are diffusions or ion implantations into a substrate or epitaxial layer.

12. The high-voltage MOS transistor of claim 11 wherein,

said extended drain region and the top layer of material are formed by using the same mask (self alignment).

13. The high-voltage MOS transistor of claim 3 wherein,

the material on which the extended drain region is formed is a substrate; and

the substrate is of one conductivity-type material, and further including a complementary transistor embedded in a well or epi-island of opposite conductivity-type material on the same substrate.

14. The complementary pair of high-voltage MOS transistors of claim 13 wherein,

the well in which the complementary transistor is embedded is the same diffusion as the extended drain for the other transistor.

15. The complementary pair of high-voltage MOS transistors of claim 14 wherein,

the well is an n-well and further used for a low voltage p-channel device.

16. The high-voltage MOS transistor of claim 2 wherein,

the top layer is floating.

17. The high-voltage MOS transistor of claim 3 wherein,

the source region and the drain region are formed in a similar manner.

18. The high-voltage MOS transistor of claim 3 further including,

low voltage logic and analog function on the same chip.

Add 92

ABSTRACT OF THE DISCLOSURE

An insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same chip to form a high-voltage MOS transistor. An extended drain region is formed on top of a substrate of opposite conductivity-type material. A top layer of material having a conductivity-type opposite that of the extended drain and similar to that of the substrate is provided by ion-implantation through the same mask window as the extended drain region. This top layer covers only an intermediate portion of the extended drain which has ends contacting a silicon dioxide layer thereabove. The top layer is either connected to the substrate or left floating. Current flow through the extended drain region can be controlled by the substrate and the top layer, which act as gates providing field-effects for pinching off the extended drain region therebetween. A complementary pair of such high-voltage MOS transistors having opposite conductivity-type are provided on the same chip.

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

HIGH VOLTAGE MOS TRANSISTORS

the specification of which

[X] is attached hereto.

[ ] was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Thomas E. Schatzel Reg. No. 22,611
Douglas R. Millett Reg. No. 31,786

Address all telephone calls to Thomas E. Schatzel at telephone No. (408) 727-7077.

Address all correspondence to:

LAW OFFICES OF THOMAS E. SCHATZEL
A Professional Corporation
10211 Scott Boulevard, Suite 201
Santa Clara, California 95054-3093

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter to each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status: patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: 4/01-00 KLAS H. EKLUND

Inventor's Signature: _____ Date: 4/14/87

Residence: 243 Mistletoe Road Los Gatos, California 95030 CA

Citizenship: Finland

Post Office Address: 243 Mistletoe Road Los Gatos, California 95030

041994

Applicant or Patentee: KLAS H. EKLUND
Serial or Patent No.:
Filed or Issued:
For: HIGH VOLTAGE MOS TRANSISTORS

Attorney's Docket No.: 520-01

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) and 1.27(c) - INDEPENDENT INVENTOR

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention entitled HIGH VOLTAGE MOS TRANSISTORS described in

[X] the specification filed herewith
[ ] application serial no. _____, filed _____
[ ] patent no. _____, issued _____.

I have not assigned, granted, conveyed or licensed and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who could not be classified as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

[X] no such person, concern, or organization
[ ] persons, concerns or organizations listed below*

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

FULL NAME n/a
ADDRESS
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

FULL NAME n/a
ADDRESS
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

FULL NAME n/a
ADDRESS
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF INVENTOR	NAME OF INVENTOR	NAME OF INVENTOR
KLAS H. EKLUND		
Signature of Inventor	Signature of Inventor	Signature of Inventor
4/17/87		
Date	Date	Date

041994

KLAS H. EKLUND

SS-520-01

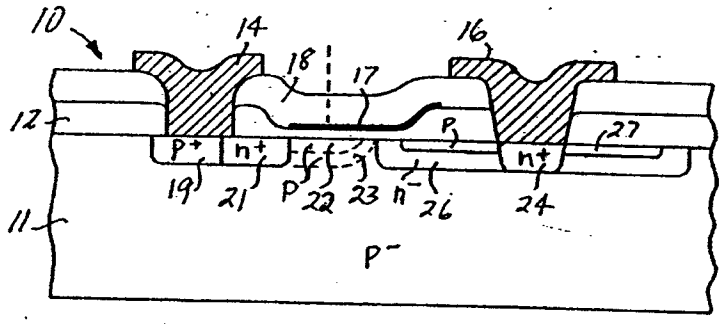

Fig. 1

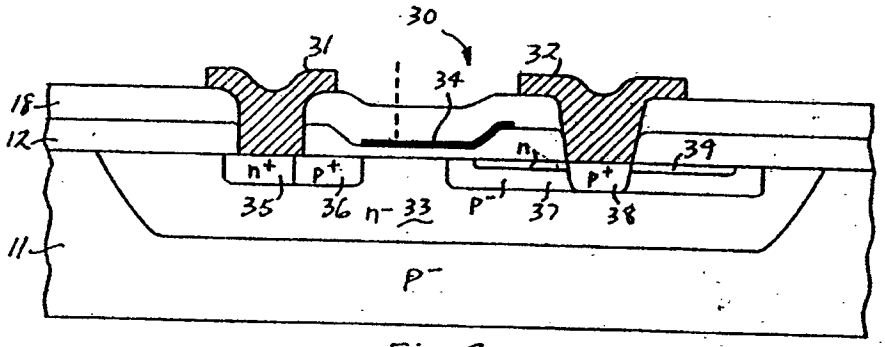

Fig. 2

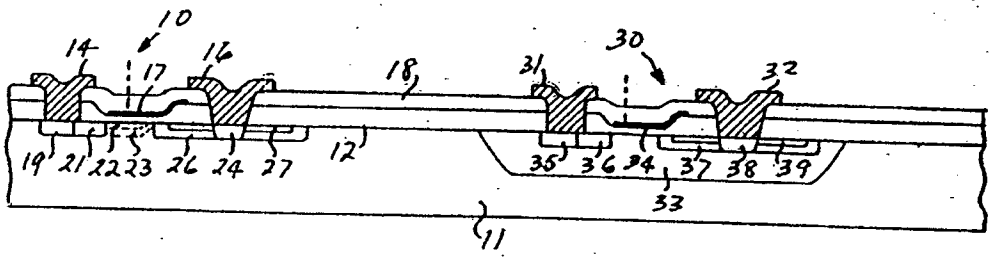

Fig. 3

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KLAS H. EKLUND

SS-520-01

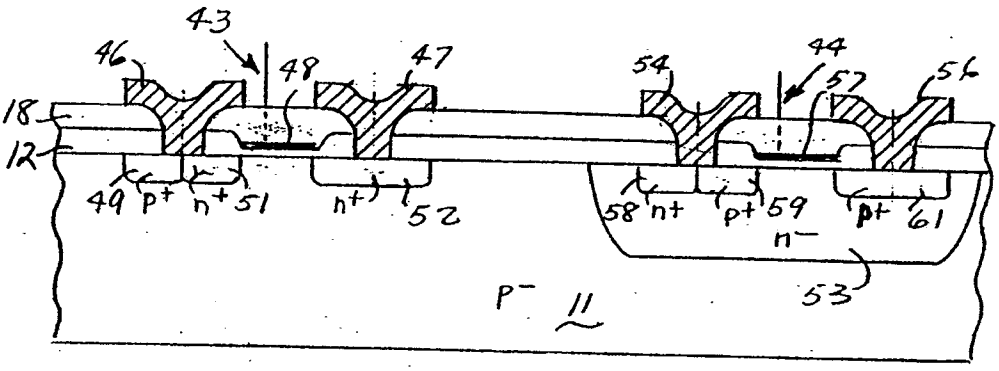

Fig_4

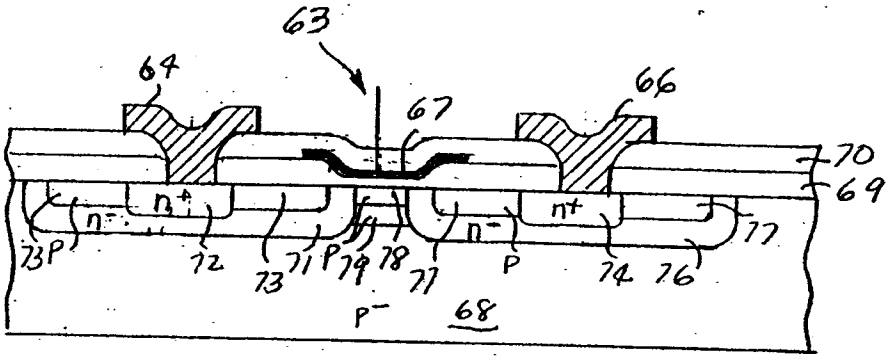

Fig_5

357/43
Jackson
KLAS H. EKLUND

Print Of Drawing
As Original Filed

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55-520-01

Conventional NLDS

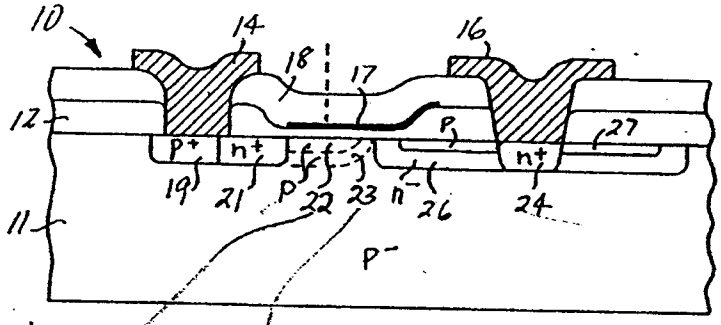

Fig-1

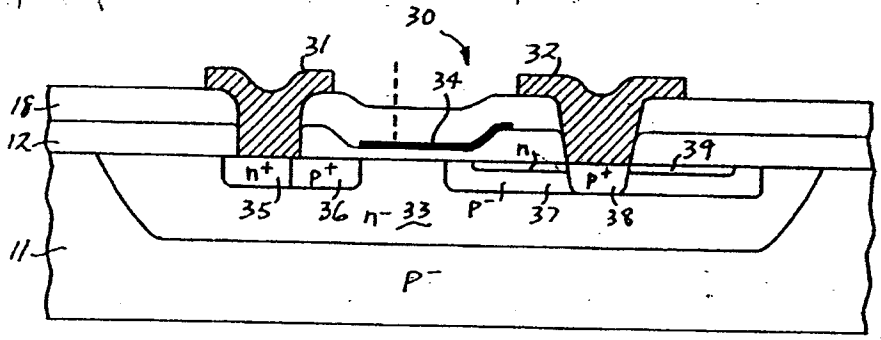

Fig-2

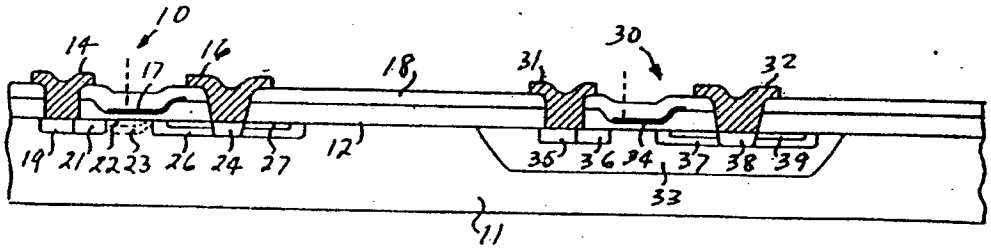

Fig 3

Print Of Drawing
As Original Filed

KLAS H. EKLUND

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2 OF 2
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SS-520-01

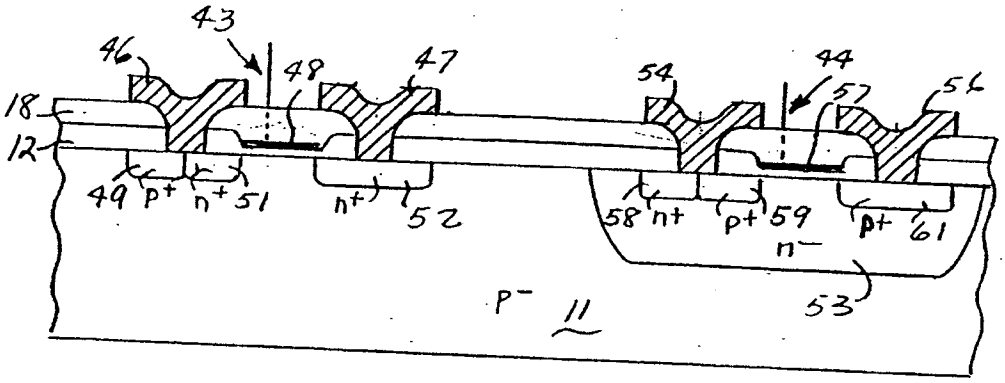

Fig-4

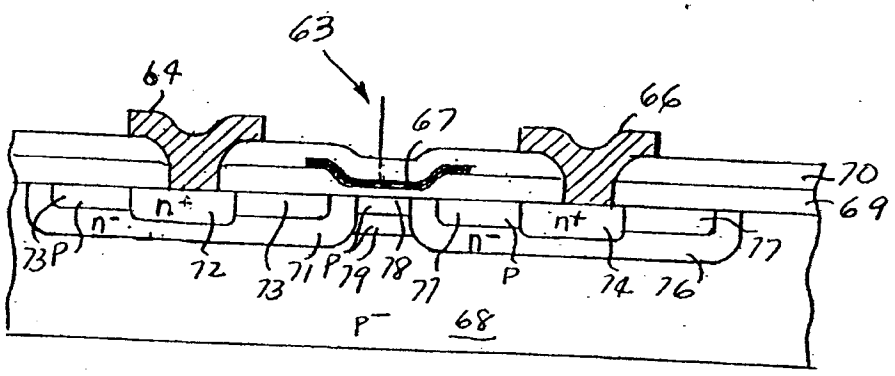

Fig-5

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/041,994	04/24/87	ERLUND K	59-320-01

THOMAS E. SCHATZEL
3211 SCOTT BLVD., STE. 201
SANTA CLARA, CA 95054-3093

EXAMINER	
JACKSON JR/D	
ART UNIT	PAPER NUMBER
253	2

DATE MAILED: 12/07/87

This is a communication from the examiner in charge of your application.

COMMISSIONER OF PATENTS AND TRADEMARKS

☐ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), — days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☒ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 1-18 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1-18 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.
8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. These drawings are ☐ acceptable; ☐ not acceptable (see explanation).
10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved. ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO EFFECT DRAWING CHANGES", PTO-1474.
12. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

PTOL-326 (Rev. 7-82) EXAMINER'S ACTION

On page 9 line 28 "72" should be --73--.

Claims 1, 2, 4-7, 16 are rejected under 35 U.S.C. 112, first and second paragraphs, as the claimed invention is not described in such full, clear, concise and exact terms as to enable any person skilled in the art to make and use the same, and/or for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The structure of claim 1 is indefinite. The language "being united in one structure" is vague and indefinite and does not clearly or concretely define the structure of applicant's invention. The terms "insulated gate FET" and "double sided JFET" are also broad and do not define applicant's invention. Claim 2 is confusing since lines 14-17 mimic lines 17-20. The other claims are rejected for dependence on 1 or 2.

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP 608.01(o). Correction of the following is required: there is no proper antecedent in the specification for the process descriptions of claims 11, 13, 14, 17.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless-

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international

application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-3, 5-9, 11, 12, 16 rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103 as obvious over Colak.

Colak shows a DMOS device wherein layer 16 may perform the function of a JFET gate "on top of" an extended drain region 14 in the embodiment of figs. 2B or 2C. Substrate layer 12 may act as the other gate of the JFET. Clearly claim 1 does not distinguish over Colak. Note that mere labels as "JFET" do not structurally distinguish the claims over Colak since the structure of Colak may be labeled an IGFET in series with a double sided JFET as shown above. Claim 2 also does not distinguish over Colak since the claimed structure is shown in Colak and the intended use language "whereby current flow..." in claim 2 does not structurally distinguish over Colak and furthermore Colak's device may perform the same intended function. See In re Pearson 181 USPQ 642 or Ex parte Minks 169 USPQ 120 on statements of intended use in claims drawn to structure as we have here. Similarly claim 3 does not distinguish over Colak. Claim 5 is a product by process claim which does not structurally distinguish applicant's final product over Colak.

A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re

Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by Process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

Claim 6 also is undistinguishing over Colak since the thickness of layer 16 is a design variable and 1 micron thickness would not be unobvious to one of ordinary skill in view of Colak. Similarly, in re claim 7 a dopant density of greater than $5x10^{16}$/cc would not be unobvious for the doping density of layer 16 of Colak. Claims 8, 9 also are obvious over Colak. Claims 11, 12 are product by process claims which also do not distinguish the final product over Colak. Claim 16 also does not distinguish over Colak as "floating" is vague and undistinguishing.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at

the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claims 4, 10, 13-15, 17 and 18 rejected under 35 U.S.C. 103 as being unpatentable over Colak in view of Thomas.

Thomas shows the obvious of providing low voltage and high voltage devices on the same substrate. It would be obvious from Thomas to practice Colak as CMOS or with other devices. Claim 4 is hence obvious. In re claims 10, 13, 15 "well" regions are also obvious from Thomas. Claims 14, 17 also are product by process claims which do not distinguish the final product over the suggestions of the references on final structure. Claim 18 also does not distinguish over the suggestions of Colak in view of Thomas.

Any inquiry concerning this communication should be directed to J. Jackson at telephone number 703-557-4824.

Jackson/EW
12-2-87

ANDREW J. JAMES
SUPERVISORY PATENT EXAMINER
GROUP ART UNIT 253

PTO - 948 (Rev. 8-82)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTACHMENT TO PAPER NUMBER 2

GROUP 260

S.N. 41994

NOTICE OF PATENT DRAWINGS OBJECTION

Drawing Corrections and/or new drawings may only be submitted in the manner set forth in the attached letter, "Information on How to Effect Drawing Changes" PTO-1474.

A. ☒ The drawings, filed on 1/24/97, are objected to as informal for reason(s) checked below:

1. ☐ Lines Pale.
2. ☐ Paper Poor.
3. ☒ Numerals Poor.
4. ☒ Lines Rough and Blurred. 6/6/1-5
5. ☐ Shade Lines Required.
6. ☐ Figures Must be Numbered.
7. ☐ Heading Space Required.
8. ☐ Figures Must Not be Connected.
9. ☐ Criss-Cross Hatching Objectionable.
10. ☐ Double-Line Hatching Objectionable.
11. ☐ Parts in Section Must Be Hatched.
12. ☐ Solid Black Objectionable.
13. ☐ Figure Legends Placed Incorrectly.
14. ☐ Mounted Photographs.
15. ☒ Extraneous Matter Objectionable. [37 CFR 1.84 (1)] BORDER LINES
16. ☐ Paper Undersized; either 8½" x 14", or 21.0 cm. x 29.7 cm. required.
17. ☐ Proper A4 Margins Required:
    ☐ TOP 2.5 cm. ☐ RIGHT 1.5 cm.
    ☐ LEFT 2.5 cm. ☐ BOTTOM 1.0 cm.
18. ☐ Other:

B. ☒ The drawings, submitted on 1/24/97, are so informal they cannot be corrected. New drawings are required. Submission of the new drawings MUST be made in accordance with the attached letter.

TO SEPARATE, HOLD TOP AND BOTTOM EDGES, SNAP–APART AND DISCARD CARBON

FORM PTO-892 (REV. 3-78) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

NOTICE OF REFERENCES CITED

SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
041994	253	2

APPLICANT(S): Eklund

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A	4626879	12/86	Colak	357	23.8	12/87
	B	4628341	12/86	Thomas	357	23.8	9/85
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG	PERTINENT PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	
S	
T	
U	

EXAMINER	DATE
J. Jackson	11/87

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)

#75.00 - 216 - #253

PATENT

Case Docket No. SS1620-01

Date April 7, 1988

In re application of: Klas H. Eklund

Serial No.: 07/041,994

Filed: April 24, 1987

For: HIGH VOLTAGE MOS TRANSISTORS

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment in the above-identified application.

[ ] No additional fee is required.

[X] Two Month Extension Fee Enclosed. ($85.00)

[ ] Additional fee calculated as follows:

CLAIMS AS AMENDED						
	Claims remaining after amendment		Highest number previously paid for	Present extra	Rate	Addtnl. Fee
Total Claims	_____	Minus	_____ =	_____ x	$12.00	= _____
Indep. Claims	_____	Minus	_____ =	_____ x	$34.00	= _____

Additional Fee Due $ _____

[X] A verified statement claiming small entity status X has been filed; _____ is attached. The fee due is fifty percentum of the above.

Fee Due $ _____

[X] A check in the amount of $ 85.00 is attached. (Two Month Extension Fee)

[X] Any additional fees may be charged to Deposit Account No. 19-0310. A duplicate of this transmittal is attached.

Respectfully submitted,

040 04/13/88 041994
Attorney For Applicant

By [signature]
Reg. No.: 22,611

Law Offices of THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard Suite 201
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Thomas E. Schatzel
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[signature] 4/7/88
Signature Date

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Klas H. Eklund

Serial No.: 07/041,994

Filed : 04-24-87

For : HIGH VOLTAGE MOS TRANSISTORS

Group Art Unit: 253

Examiner: J. Jackson

Attorneys Docket No.: SS-520-01

COMMISSIONER OF PATENTS & TRADEMARKS
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Date of this Paper:

April 7, 1988

AMENDMENT

In response to the U.S. Patent Office Action mailed December 7, 1987 (Paper No. 2), please amend this application as follows:

In the Specification

Page 1, line 26, change "of" to --on--;

Page 9, line 15, insert the following paragraph:

--It should be noted that the term "substrate" refers to the physical material on which a microcircuit is fabricated. If a transistor is fabricated on a well of n or p type material within a primary substrate of opposite type material, the well material can be considered a secondary substrate. Similarly, if a transistor is fabricated on an epitaxial layer or epi-island that merely supports and insulates the transistor, the epitaxial layer or epi-island can be considered a secondary substrate. An epi-island is a portion of an epitaxial layer of one conductivity type that is isolated from the remaining portion of the epitaxial layer by diffusion pockets of an opposite conductivity type. When complimentary transistors are formed on the same chip, the well in which one complimentary transistor is embedded is formed by the same diffusion as the extended drain region for the other transistor.--.

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Page 9, line 28, change "72" to --73--.

In the Claims

Cancel claims 1-5 and 8-18.

Add new claims 19-23 as follows:

19. A high voltage MOS transistor comprising:

a semiconductor substrate of a first conductivity type having a surface,

a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,

a source contact connected to one pocket,

a drain contact connected to the other pocket,

an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,

a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage,

an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.